AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (original) A laminated capacitor comprising:

a capacitor body having first and second major surfaces and including a laminated stack of a plurality of dielectric layers, at least a pair of a first and second internal electrodes opposed to each other with at least one of the dielectric layers being disposed therebetween;

a plurality of first feedthrough conductors perforating through at least one of the dielectric layers provided within the capacitor body, the first feedthrough conductors being electrically insulated from the second internal electrodes and electrically connected to the first internal electrodes; and

a plurality of second feedthrough conductors perforating through the capacitor body and provided within the capacitor body, the second feedthrough conductors are electrically insulated from the first internal electrodes and are electrically connected to the second internal electrodes, the first and second feedthrough conductors are arranged to offset the magnetic fields induced by the electric current flowing through the internal electrodes;

a plurality of first external terminal electrodes arranged so as to correspond to the respective first feedthrough conductors and electrically connected to respective ones of the first feedthrough conductors; and

a plurality of second external terminal electrodes, which are arranged to correspond to respective ones of the second feedthrough conductors and electrically connected to respective ones of the second feedthrough conductors; wherein

the first external terminal electrodes are located at least on the first major surface of the capacitor body and extend substantially parallel to the internal electrodes, and the second external terminal electrodes are located on both the first major surface and the second major surface in opposed relation to the first major surface.

Claim 2 (original) A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 2×10^{-3} mm^2.

Claim 3 (original) A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

Claim 4 (original) A laminated capacitor according to Claim 1, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

Claim 5 (original) A laminated capacitor according to Claim 1, wherein the first external terminal electrodes are disposed on both the first major surface and the second major surface of the capacitor body.

Claim 6 (original) A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross sectional area of at least about 2×10^{-3} mm^2.

Claim 7 (original) A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

Claim 8 (original) A laminated capacitor according to Claim 5, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

Claim 9 (original) A laminated capacitor according to Claim 1, wherein solder bumps are provided on the first and second external terminal electrodes.

Claim 10 (original) A laminated capacitor according to Claim 1, wherein the laminated capacitor defines a decoupling capacitor.

Claim 11 (original) A wiring connection structure of a decoupling capacitor to be connected to a power supply circuit for a MPU chip provided in a microprocessing unit, the decoupling capacitor comprising:

a capacitor body having first and second major surfaces opposed to each other;

feedthrough conductors disposed within the capacitor body and arranged to perforate from the first major surface to the second major surface; and

at least one of power supply lines and signal lines connected to the MPU chip are grounded to a mother board via the feedthrough conductors.

Claim 12 (original) A wiring connection structure of a decoupling capacitor according to Claim 11, wherein the decoupling capacitor includes:

a capacitor body having first and second major surfaces and including a laminated stack of a plurality of dielectric layers, at least a pair of a first and second internal electrodes opposed to each other with at least one of the dielectric layers being disposed therebetween;

a plurality of first feedthrough conductors perforating through at least one of the dielectric layers provided within the capacitor body, the first feedthrough conductors being electrically insulated from the second internal electrodes and electrically connected to the first internal electrodes; and

a plurality of second feedthrough conductors perforating through the capacitor body and provided within the capacitor body, the second feedthrough conductors are electrically insulated from the first internal electrodes and are electrically connected to the second internal electrodes, the first and second feedthrough conductors are arranged to offset the magnetic fields induced by the electric current flowing through the internal electrodes;

a plurality of first external terminal electrodes arranged so as to correspond to the respective first feedthrough conductors and electrically connected to respective ones of the first feedthrough conductors; and

a plurality of second external terminal electrodes, which are arranged to correspond to respective ones of the second feedthrough conductors and electrically connected to respective ones of the second feedthrough conductors; wherein

the first external terminal electrodes are located at least on the first major surface of the capacitor body and extend substantially parallel to the internal electrodes, and the second external terminal electrodes are located on both the first major surface and the second major surface in opposed relation to the first major surface .

Claim 13 (original) A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 2×10^{-3} mm^2.

Claim 14 (original) A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

Claim 15 (original) A wiring connection structure of a decoupling capacitor according to Claim 12, wherein at least one of the second feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

Claim 16 (original) A wiring connection structure of a decoupling capacitor according to Claim 12, wherein the first external terminal electrodes are disposed on both the first major surface and the second major surface of the capacitor body.

Claim 17 (original) A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross sectional area of at least about 2×10^{-3} mm^2.

Claim 18 (original) A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 7×10^{-3} mm^2.

Claim 19 (original) A wiring connection structure of a decoupling capacitor according to Claim 16, wherein at least one of the first feedthrough conductors has a cross-sectional area of at least about 1.5×10^{-2} mm^2.

Claim 20 (original) A wiring connection structure of a decoupling capacitor according to Claim 12, wherein solder bumps are provided on the first and second external terminal electrodes.

Claims 21-24 (canceled)